

A cross-sectional view of a semiconductor device. It features a central square region labeled "P+" (P-type) and "N+" (N-type). This central region is surrounded by a square frame. The frame is composed of several layers: an innermost square labeled "112", a middle square labeled "114", and an outermost square labeled "108". The region between the innermost and middle squares is labeled "117". The region between the middle and outermost squares is labeled "106". The region between the outermost square and the central P+ region is labeled "104". The region between the outermost square and the central N+ region is labeled "102". A vertical arrow labeled "1A" points upwards on the left side of the device.

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Title Self-Aligned Trench Mosfets and
Methods for Making the Same
Inventor: Duc Chau, et al.
Docket No. 11948.3

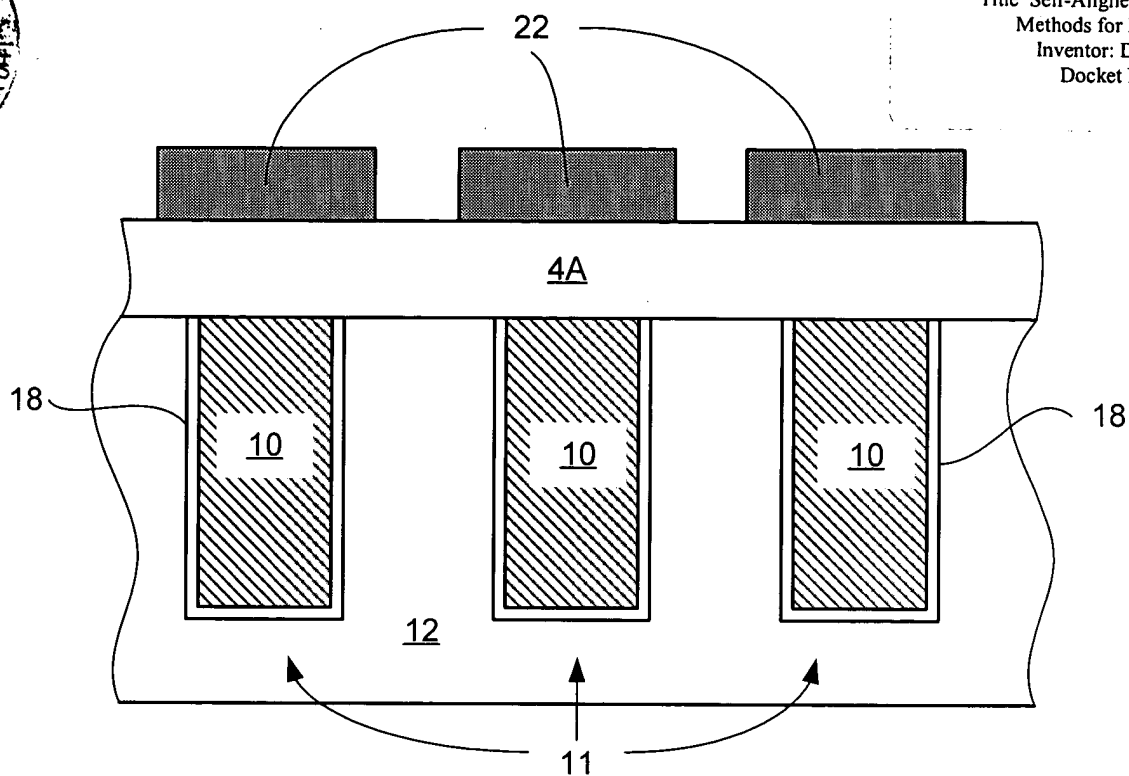


Figure 3

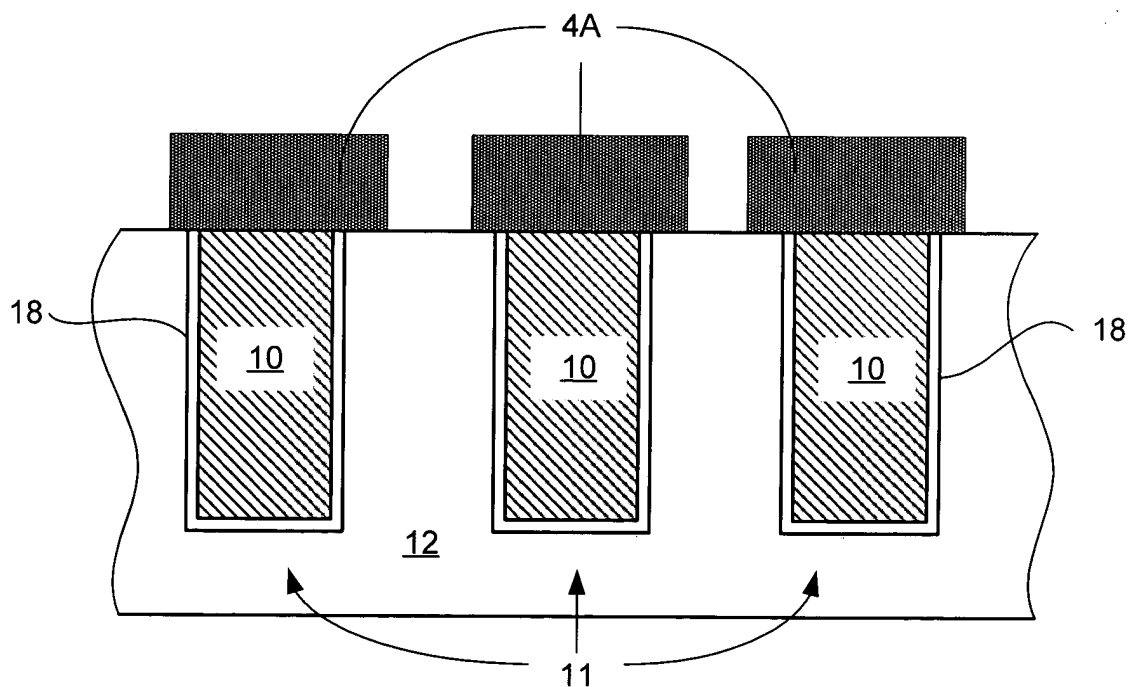


Figure 4



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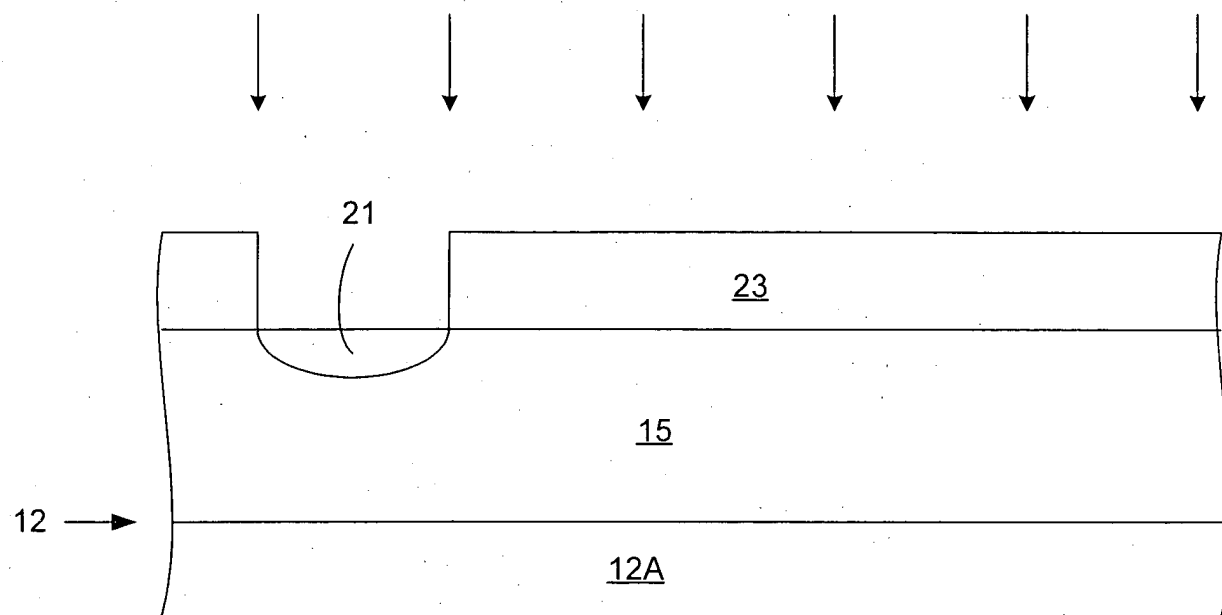


FIGURE 5

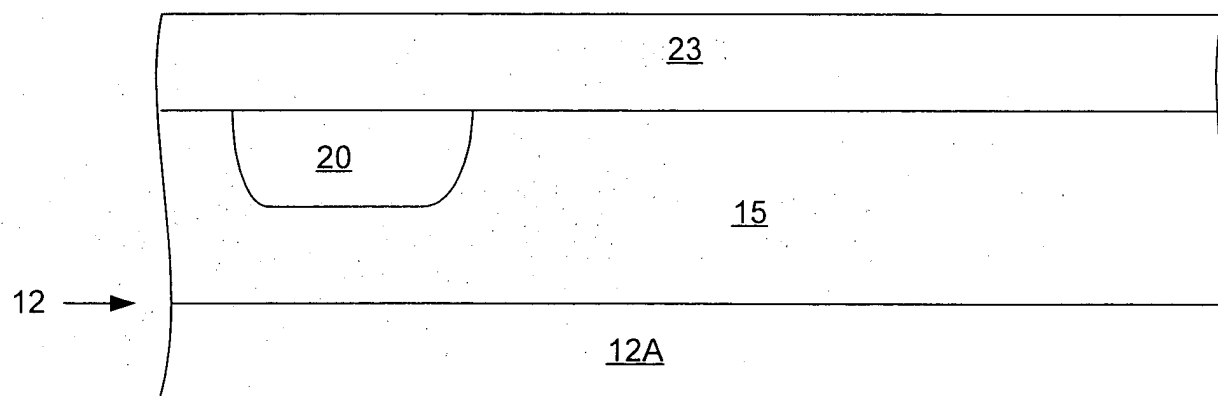


FIGURE 6

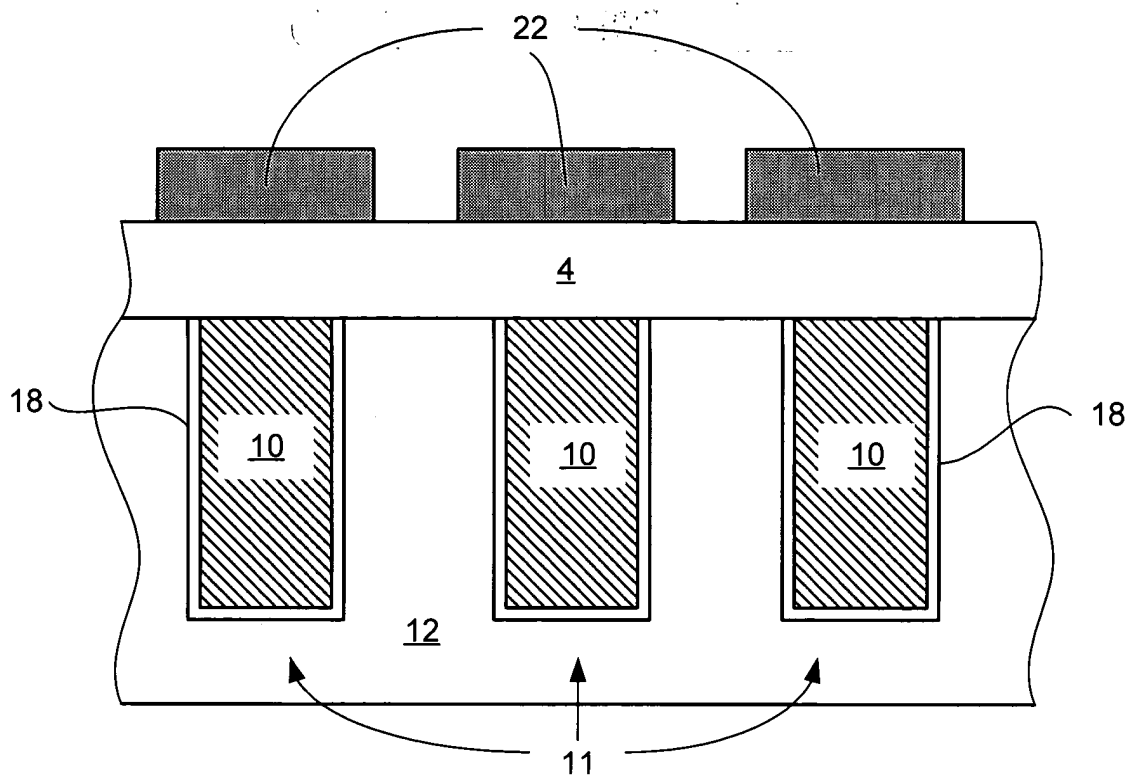


Figure 3

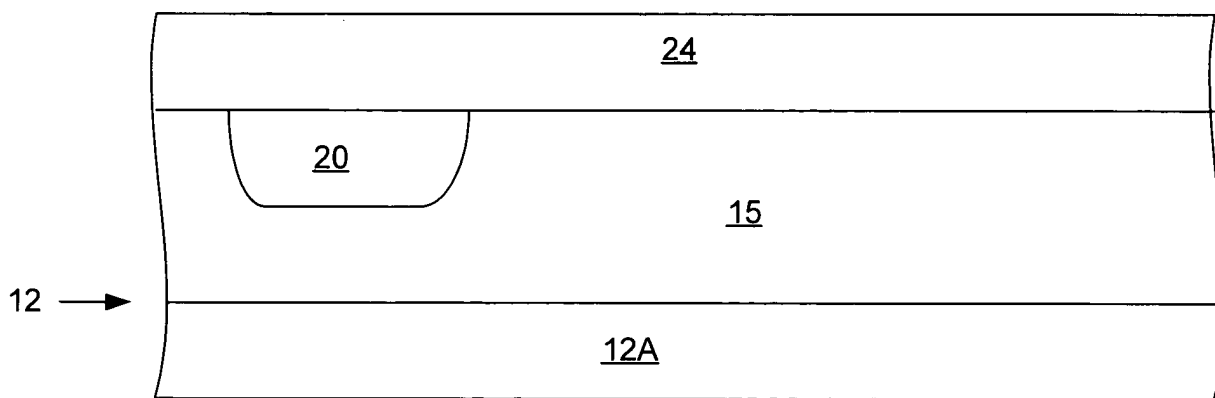


FIGURE 6



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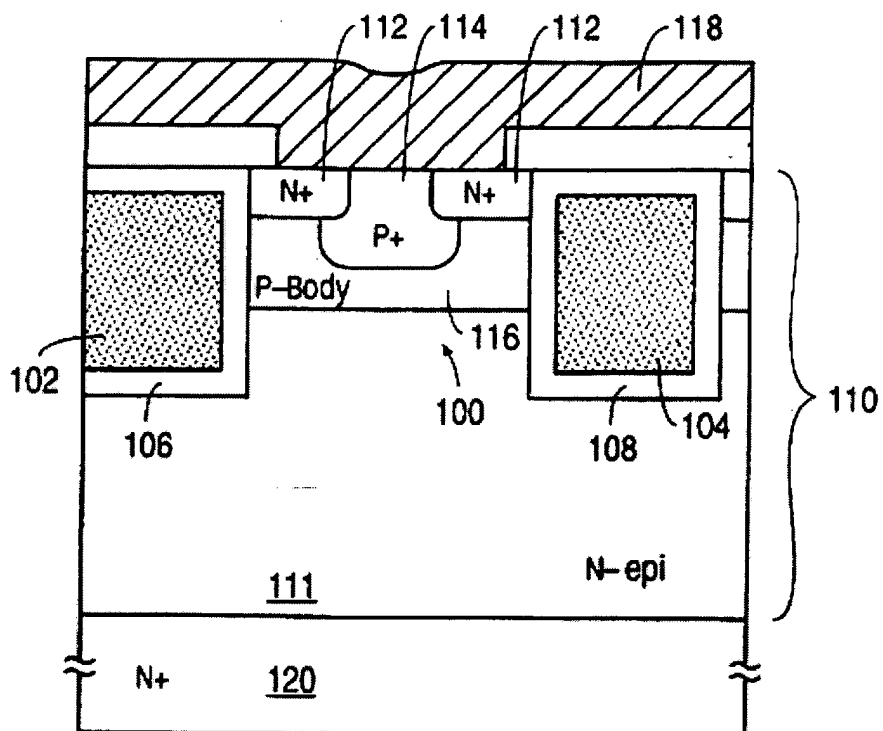


FIGURE 1
(PRIOR ART)